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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,088	08/15/2001	Eugene W. Lee	3981-6	2875

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EXAMINER	
DAVIS, ZACHARY A	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,088	LEE ET AL.	
	Examiner	Art Unit	
	Zachary A Davis	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20020404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 56 (see page 6, line 14 of the specification).

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 88 (see Figure 7).

3. The drawings are objected to because they include typographical and other errors. Specifically, Figure 4 includes the label "Scambler Polynomial"; it appears this is intended to read "Scrambler Polynomial". Further, in Figure 8, it appears that the arrows indicating the flow of data between elements 104 and 112 and between elements 116 and 108 indicate the incorrect direction when read in the context of page 7, lines 22-25 and page 8, lines 6-9 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary,

the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitations "the output data register" and "the new seed register" in line 19. There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Walker et al, US Patent 6862701.

In reference to Claim 1, Walker discloses a scrambler device that scrambles a parallel array of input bits into an array of scrambled output bits during the same clock period (column 15, lines 39-42).

In reference to Claim 2, Walker further discloses a new seed register for storing the scrambled output bits from a previous clock period and supplying the scrambled output bits to apply to the array of input bits during the current clock period (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254).

In reference to Claim 3, Walker further discloses generating an array of polynomial values for applying to the array of input bits through feedback of previously generated scrambled output bits (column 15, lines 39-42; see Figure 7).

In reference to Claim 4, Walker further discloses a seed register (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254).

In reference to Claim 5, Walker further discloses selecting the scrambled output bits for applying to the input bits according to a polynomial value, a bit length, and a bit position (column 15, lines 39-42; column 16, lines 12-50; see Figure 7).

In reference to Claim 6, Walker further discloses that a 1+X(39)+X(58) scramble polynomial is applied to each bit (column 15, lines 39-42). Walker also discloses the specific polynomial values based on the connections illustrated in Figure 7 and described in column 16, lines 12-50.

In reference to Claim 7, Walker further discloses an input register that outputs the parallel array of input bits to the scrambler (Figure 7, note input I; also note, for example, Figure 4, Encoder 50 which provides input to the scrambler) and an output register that receives the array of scrambled output bits from the scrambler (Figure 7, note output O; also note, for example, Figure 4, Frame Assembler 34 which receives output from the scrambler).

In reference to Claim 8, Walker further discloses that the output of the scrambler device is coupled to the new seed register (see Figure 7).

In reference to Claims 9 and 10, Walker further discloses that the scramblers are used to scramble an array of input bits from network packets (column 9, lines 37-49; column 10, lines 5-10).

In reference to Claim 11, Walker discloses a method including receiving a parallel array of input bits (see Figure 7, input I), storing an array of previously scrambled output bits from a previous clock period (Figure 7, scrambler register 254; column 15, line 66-column 6, line 6), and applying the previously scrambled bits to the input bits during a current clock period to generate a current array of scrambled output bits (column 15, lines 39-42; column 16, lines 12-50; see Figure 7).

In reference to Claim 12, Walker further discloses storing the previously scrambled bits as new seed values (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254).

In reference to Claim 13, Walker further discloses selecting the new seed values according to a polynomial value, a bit length, and a bit position (column 15, lines 39-42; column 16, lines 12-50; see Figure 7).

In reference to Claim 14, Walker further discloses that a 1+X(39)+X(58) scramble polynomial is applied to each bit (column 15, lines 39-42).

In reference to Claims 15 and 16, Walker further discloses that a de-scrambler can be made by rearranging the scrambler (see column 17, lines 36-42).

In reference to Claims 17 and 18, Walker further discloses de-scrambling scrambled packet bits received over a network and scrambling parallel arrays of packet bits before sending over a network (column 9, lines 44-49; column 10, lines 5-12 and 18-24).

In reference to Claim 19, Walker discloses a device including an ingress circuit for processing packets received over a network (Figure 4, receiver 122; column 9, lines 37-49), an egress circuit for processing packets for sending over the network (Figure 4, transmitter 120; column 9, lines 44-49), a fabric for transferring packets between the ingress and egress circuits (Figure 4, bus 18 and 19; see also column 1, lines 38-44), and a scrambler circuit that scrambles a parallel array of input bits into an array of scrambled output bits during the same clock period (column 15, lines 39-42).

In reference to Claims 20 and 21, Walker further discloses a new seed register for storing the scrambled output bits from a previous clock period and supplying the scrambled output bits to apply to the array of input bits during the current clock period (column 15, line 66-column 16, line 6; Figure 7, scrambler register 254).

In reference to Claims 22-24, Walker further discloses that a de-scrambler can be made by rearranging the scrambler (see column 17, lines 36-42).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Powell et al, US Patent 5031129, discloses a parallel pseudo-random generator.

b. Lee et al, US Patent 5241602, discloses an interleaved parallel scrambling system.

c. Nishida et al, US Patent 5844989, discloses a data scrambling apparatus operating in parallel using a polynomial scrambling function.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zachary A Davis whose telephone number is (571) 272-3870. The examiner can normally be reached on weekdays 8:30-6:00, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Caldwell can be reached on (571) 272-3868. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Caldwell

ZAD
zad

ANDREW CALDWELL
SUPERVISORY PATENT EXAMINER